

What is claimed is:

1. A method of fabricating a semiconductor device, comprising:
forming a conductive region at the top of a semiconductor substrate;
forming a first interlayer dielectric layer on the semiconductor substrate over the entirety of the conductive region;
forming a conductive line, which is to be connected to the conductive region, on the first interlayer dielectric layer;
forming a second interlayer dielectric layer on the conductive line;
removing portions of the first interlayer dielectric layer, conductive line, and second interlayer dielectric layer which overlie the conductive region to form a contact hole which exposes the conductive region; and
filling the contact hole with a conductive material to connect the conductive line to the conductive region.

2. The method of claim 1, wherein said removing of portions of the first interlayer dielectric layer, conductive line, and second interlayer dielectric layer comprises:

forming a patterned photosensitive film on the second interlayer dielectric layer, the patterned photosensitive film defining an opening therein having a width that is greater than the critical dimension of the conductive line,

etching the second interlayer dielectric layer using the photosensitive film pattern as an etch mask until the conductive line is exposed, and

etching the conductive line and the first interlayer dielectric layer using the etched second interlayer dielectric layer as an etch mask.

3. The method of claim 2, wherein the etching of the conductive line and the first interlayer dielectric layer comprises:

etching the conductive line using the etched second interlayer dielectric layer as an etch mask to expose the first interlayer dielectric layer, and
then discretely etching the exposed first interlayer dielectric layer.

4. The method of claim 2, wherein the etching of the second interlayer dielectric layer comprises an anisotropic etching process which produces inclined

3 sidewalls therein, whereby the cross-sectional area of an upper portion of the
4 contact hole is greater than that of a lower portion thereof.

1 5. The method of claim 3, wherein the etching of the second interlayer
2 dielectric layer comprises an anisotropic etching process which produces inclined
3 sidewalls therein, whereby the cross-sectional area of an upper portion of the
4 contact hole is greater than that of a lower portion thereof.

1 6. The method of claim 2, and further comprising removing the
2 photosensitive film pattern before the conductive line is etched.

1 7. The method of claim 3, and further comprising removing the
2 photosensitive film pattern before the conductive line is etched.

3 8. The method of claim 1, wherein the forming of the conductive line
4 comprises:
5 forming a dielectric film pattern defining a line-shaped opening on the first
6 interlayer dielectric layer, and
7 depositing conductive material in the line-shaped opening.

8 9. A method of fabricating semiconductor devices, comprising:
9 forming a conductive region at the top of a semiconductor substrate;
10 forming a first interlayer dielectric layer on the semiconductor substrate over
11 the entirety of the conductive region;

12 forming a conductive line, which is to be connected to the conductive region,
on the first interlayer dielectric layer, the conductive line having a gap therein of a
predetermined width;

forming a second interlayer dielectric layer on the conductive line such that a
first portion of the second interlayer dielectric layer occupies the gap in the
conductive line;

removing a portion of the first interlayer dielectric layer overlying the
conductive region, the first portion of the second interlayer dielectric layer occupying

the gap in the conductive line, and a second portion of the second interlayer dielectric layer overlying the gap to form a contact hole; and

filling the contact hole with a conductive material to connect the conductive line to the conductive region.

10. The method of claim 9, wherein the of removing portions of the first and second interlayer dielectric layers comprises:

forming a photosensitive film pattern on the second interlayer dielectric layer, the photosensitive film pattern defining an opening therein having widths, in two orthogonal X and Y directions, that are greater than the critical dimension of and the width of the gap in the conductive line, respectively, and

etching the second portion of the second interlayer dielectric layer, the first portion of the second interlayer dielectric layer occupying the gap in the conductive line, and a portion of the first interlayer dielectric layer underlying the gap in the conductive line, using the photosensitive film pattern and the conductive line as etch masks.

11. The method of claim 9, wherein the etching of the first and second interlayer dielectric layers comprises:

etching the second portion of the second interlayer dielectric layer using the photosensitive film pattern as an etch mask until a portion of the conductive line defining the gap is exposed, and

etching the first portion of the second interlayer dielectric layer occupying the gap in the conductive line, and the portion of the first interlayer dielectric layer underlying the gap, using the etched second interlayer dielectric layer and the portion of the conductive line defining the gap therein as etch masks.

12. The method of claim 9, wherein the etching of the portion of the conductive line defining the gap therein comprises an anisotropic etching process which produces inclined sidewalls therein, whereby the cross-sectional area of an upper portion of the contact hole is greater than that of a lower portion thereof.

1 13. The method of claim 10, wherein the etching of the portion of the
2 conductive line defining the gap therein comprises an anisotropic etching process
3 which produces inclined sidewalls therein, whereby the cross-sectional area of an
4 upper portion of the contact hole is greater than that of a lower portion thereof.

1 14. The method of claim 11, further comprising removing the
2 photosensitive film pattern after the portion of the conductive line defining the gap
3 therein is exposed.

1 15. The method of claim 9, wherein the forming of the conductive line
2 comprises:

3 forming a dielectric film pattern having a line-shaped opening on the first
4 interlayer dielectric layer; and

5 depositing conductive material within the line-shaped opening.

1 16. A semiconductor device having a conductive region, a conductive line,
2 and a contact plug having an upper portion, sidewalls and a lower portion defining
3 the bottom thereof, the conductive line being electrically connected to the conductive
4 region via the sidewalls of the contact plug, the conductive region being electrically
5 connected to the conductive line via the bottom of the contact plug, and the cross-
6 sectional area of the contact plug decreasing in a direction extending from the upper
7 portion of the contact plug to the lower portion thereof.

1 17. The semiconductor device of claim 16, wherein the lower portion of the
2 contact plug is self aligned with the critical dimension of the conductive line.

1 18. The semiconductor device of claim 16, wherein the width of the upper
2 portion of the contact plug, as taken in the width-wise direction of the conductive
3 line, is greater than the critical dimension of the conductive line.

1 19. The semiconductor device of claim 16, wherein the conductive region
2 is one of a bit line contact pad, a word line contact pad, a source region, a drain
3 region, a gate electrode, and an interlayer wiring.

1 20. The semiconductor device of claim 16, wherein the conductive line is
2 one of a bit line, a word line, and an interlayer wiring.

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